25 Spring ECEN 720: High-Speed Links: Circuits and Systems Pre-lab Report

Lab2: Channel Models

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**Pre-Lab**

1. Plot S11 and S21 for the circuit shown in Figure 10 using Cadence (RT=50Ω).

a. Td=0ps (no t-line), C1=0pF, L1=0nH, C2=1pF

b. Td=0ps (no t-line), C1=3pF, L1=2nH, C2=1pF

c. Td=300ps , C1=3pF, L1=2nH, C2=1pF

Comment on the results.

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| **S-Parameter** | **Definition** | **Physical Meaning** |
| S11 | b1/a1 | Input Reflection Coefficient (Return Loss at Port 1) |
| S22 | b2/a2 | Output Reflection Coefficient (Return Loss at Port 2) |
| S21 | b2/a1 | Forward Transmission (Insertion Loss, Gain, or Attenuation from Port 1 to Port 2) |
| S12 | b1/a2 | Reverse Transmission (Isolation or Reverse Gain from Port 2 to Port 1) |

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| Case1  For low frequence C= open, no reflection RS = RT  For high frequency C= short, reflection=-1 RT=0 |
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| Case 2  Same condition with case1 with LC in the middle (bandpass filter will have high transmission at certain frequencies and may produce large reflections at other frequencies.) |
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| Case 3  transmission line adds signal delay, but even without this wire, the LC element will still affect the impedance match, causing reflections to exist. |

* In high-frequency circuits, even if there are no transmission lines, impedance matching design still needs to be considered to reduce reflections and improve signal integrity (SI).

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| Feature | AC Coupled Termination | DC Coupled Termination |
| Definition | Uses a **capacitor** in series to block DC components while allowing AC signals to pass. | Direct electrical connection without capacitive isolation, passing both AC and DC components. |
| DC Biasing | Blocks DC, requiring separate biasing networks for proper voltage levels at the receiver. | Directly maintains DC bias from the source, simplifying circuit design. |
| Impedance Matching | Provides impedance matching only for **AC signals**. Requires external biasing resistors to maintain termination impedance. | Provides **continuous impedance matching** for both AC and DC signals, ensuring signal integrity. |
| Complexity | Requires additional biasing networks, making design **more complex**. | Simpler implementation since no additional biasing is needed. |
| Common Applications | High-speed digital signals (e.g., **LVDS, HDMI, PCIe, RF circuits**), where DC biasing differs between transmitter and receiver. | Low-frequency or **DC-coupled systems** (e.g., **TTL, CMOS, differential signaling like USB, DDR memory**), where maintaining DC level is crucial. |